Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A networking apparatus for providing fault tolerance to memory comprising:

a first memory including a plurality of entries to store data concerning a packet with an address information, wherein the data concerning the packet is stored in one of the entries according to the address information; and

a second memory to store a status of at least one of the entries, wherein the status indicates that whether or not the corresponding entry is defective.

[c2] 2. The networking apparatus in claim 1, wherein the data concerning the packet includes a host/port relationship.

[c3] 3. The networking apparatus in claim 1, wherein the address information includes a MAC ID of the packet.

[c4] 4. The networking apparatus in claim 3, wherein the address information includes a source ID (SID) of the packet.

[c5] 5. The networking apparatus in claim 3, wherein the address information includes a destination ID (SID) of the packet.

[c6] 6. The networking apparatus in claim 3, wherein the relationship between the address information of the packet and the corresponding entry of the first memory is determined by a hashing scheme.

[c7] 7. The networking apparatus in claim 1, wherein the first memory is a MAC address memory.

[c8] 8. The networking apparatus in claim 1, wherein the second memory is at least a register.

[c9] 9. The networking apparatus in claim 1, wherein the networking apparatus further includes a third memory to store the data concerning the packet if the entry corresponding to the packet is defective.

[c10] 10. The networking apparatus in claim 10, wherein the third memory is a content-addressable memory (CAM).

[c11] 11.A networking apparatus in claim 1 wherein the networking apparatus is a switch.

[c12] 12.A networking apparatus in claim 1 wherein the networking apparatus is a router.

[c13] 13.A method for providing fault tolerance to memory in a networking apparatus comprising:
performing a built-in self test (BIST) on a first memory

including a plurality of entries;
marking a second memory to indicate a status of at least one of the entries, wherein the status is for indicating whether the corresponding entry is defective;
finding an entry of the first memory according to an address information of a packet; and
checking the second memory to determine whether the entry corresponding to the address information of the packet is defective or not.

[c14] 14.The method in claim 13 further comprising:
broadcasting the packet if the entry corresponding to the address information of the packet is defective.

[c15] 15. The networking apparatus in claim 13, wherein the address information includes a MAC ID of the packet.

[c16] 16. The networking apparatus in claim 15, wherein the address information includes a source ID (SID) of the packet.

[c17] 17. The networking apparatus in claim 15, wherein the address information includes a destination ID (SID) of the packet.

[c18] 18. The networking apparatus in claim 13, wherein the relationship between the address information of the packet and the corresponding entry of the first memory

is determined by a hashing scheme.

[c19] 19.The method in claim 13 further comprising:
comparing the address information of the packet with a content of the corresponding entry of the first memory if the corresponding entry of the first memory is not defective;
forwarding the packet to a specific port according to the content of the corresponding entry of the first memory if the comparison yields a match; and
broadcasting the packet if the comparison does not yield a match.

[c20] 20. The method in claim 19 further comprising: storing data concerning the packet into the corresponding entry of the first memory if the comparison does not yield a match.

[c21] 21.The method in claim 13 further comprising: storing data concerning the packet in a third memory if the first memory is defective.

[c22] 22. The method in claim 21 further comprising:
comparing the data of the packet with a content of the corresponding entry of the first memory if the corresponding entry of the first memory is not defective;
comparing the data of the packet with a content of the

third memory if the corresponding entry of the first memory is defective;

forwarding the packet to a specific port according to at least one of the content of the corresponding entry of the first memory and the third memory if the comparison yields a match; and

broadcasting the packet if the comparison does not yield a match.

[c23] 23. The method in claim 24 further comprising: storing the data of the packet into the third memory if the comparison does not yield a match.